PATENT ABSTRACTS OF JAPAN

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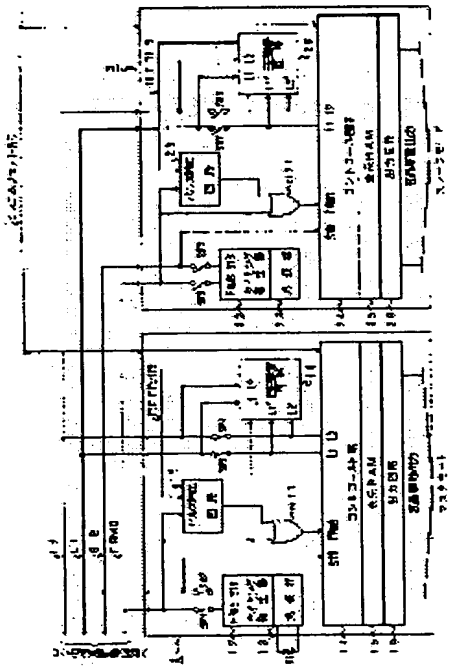
(54) LIQUID CRYSTAL DRIVING CIRCUIT AND CONTROL METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the occurrence of the blackout of a liquid crystal display by performing a synchronization without utilizing a system resetting function at the time of eliminating a synchronous deviation when the synchronous deviation is generated in the circuit.
SOLUTION: A slave mode liquid crystal driving circuit outputs gradation level signals L1', L2' from a control circuit 24 of itself to input them to a self- diagnostic circuit 28. Here, they are compared with gradation level signals L1, L2 to be inputted from the control circuit 14 of a master mode liquid crystal driving circuit as to whether L1=L1', L2=L2' or not, and when they are not matched with each other, the circuit 28 judges that a synchronous deviation is generated to invert the logic of a signal REFRHB from the circuit 28 whilst they are noncoincident. The synchronous deviation is dissolved by the inversion of the logic of the signal REFRHB. Then, the synchronous deviation is eliminated by inserting an 'H' pulse during a period when a frame signal FRMB to be inputted from the master liquid crystal driving circuit to the control circuit 24 while the logic of the signal REFRHB is inverted is an 'L'.



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CLAIMS

[Claim(s)]

[Claim 1] A master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits equipped with the control circuit in which each builds a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. The gradation level signals L1 and L2 are outputted from the self control circuit 14, and it sends out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self, and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the control approach of the liquid crystal drive circuit which cancels synchronous gap by reversal of the logic of this signal REFRHB The control approach of the liquid crystal drive circuit characterized by inserting the "H" pulse between the "L" periods of the frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and canceling synchronous gap while the logic of said signal REFRHB is reversed.

[Claim 2] A master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits equipped with the control circuit in which each builds a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB

and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. The gradation level signals L1 and L2 are outputted from the self control circuit 14, and it sends out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self', and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the control approach of the liquid crystal drive circuit which cancels synchronous gap by reversal of the logic of this signal REFRHB While the logic of said signal REFRHB is reversed, The control approach of the liquid crystal drive circuit characterized by stopping the input of said frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and liquid aforementioned ****** timing signal STB, and canceling synchronous gap.

[Claim 3] A master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits equipped with the control circuit in which each builds a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. The gradation level signals L1 and L2 are outputted from the self control circuit 14, and it sends out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self', and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit

28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the control approach of the liquid crystal drive circuit which cancels synchronous gap by reversal of the logic of this signal REFRHB Said signal REFRHB is inputted into said timing generator and control circuit of all column side liquid crystal drive circuits. The control approach of the liquid crystal drive circuit characterized by canceling synchronous gap by resetting said timing generator and said gradation level signal generator built in said control circuit.

[Claim 4] A master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits equipped with the control circuit in which each builds a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. It has a means to output the gradation level signals L1 and L2 from the self control circuit 14, and to send out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self, and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the liquid crystal drive circuit equipped with a means to cancel synchronous gap by reversal of the logic of this signal REFRHB While the logic of said signal REFRHB is reversed in said slave-mode liquid crystal drive circuit, The liquid crystal drive circuit characterized by having the amendment circuit which inserts the "H" pulse between the "L" periods of the frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and cancels synchronous gap.

[Claim 5] A master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits equipped with the control circuit in which each builds a gradation level

signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. It has a means to output the gradation level signals L1 and L2 from the self control circuit 14, and to send out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self', and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the liquid crystal drive circuit equipped with a means to cancel synchronous gap by reversal of the logic of this signal REFRHB While the logic of said signal REFRHB is reversed in said slave-mode liquid crystal drive circuit. The liquid crystal drive circuit characterized by having the amendment circuit which is made to suspend the input of said frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and liquid aforementioned ****** timing signal STB, and cancels synchronous gap.

[Claim 6] Said self-test circuit 28 is a liquid crystal drive circuit given in any of claim 4 characterized by equipping the last stage with an inverter thru/or claim 5 they are.

[Claim 7] A master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits equipped with the control circuit in which each builds a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. It has a means to output the gradation level signals L1 and L2 from the self control circuit 14, and to send out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said

liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self', and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the liquid crystal drive circuit equipped with a means to cancel synchronous gap by reversal of the logic of this signal REFRHB Said signal REFRHB is inputted into said timing generator and control circuit of all column side liquid crystal drive circuits. The liquid crystal drive circuit characterized by having a means to reset said timing generator and said gradation level signal generator built in said control circuit, and to cancel synchronous gap.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the liquid crystal drive circuit which builds in control circuits, such as Display RAM, and the display RAM address, a gradation arithmetic circuit, and its control approach about a liquid crystal drive circuit.
[0002]
[Description of the Prior Art] recent years and PDA (Personal Digital Assistants portable information terminal) etc. -- **** -- since importance is attached to low-power-ization, control circuits, such as Display RAM, and a display RAM address circuit, a gradation arithmetic circuit, are made to build in the column side liquid crystal drive circuit of a liquid crystal display, and development of the technique of attaining low-power-ization of the equipment which uses this liquid crystal display is furthered. A liquid crystal display display is performed combining the output of the liquid crystal drive circuit for a gradation display such whose a drive circuit of a liquid crystal display is a column side liquid crystal drive circuit, and the output of the Rhine selection liquid crystal drive circuit which is a low side liquid crystal drive circuit.
[0003] There are the 2 modes of a master mode and a slave mode in a column side liquid crystal drive circuit, in a master mode, a built-in oscillator is operated and a synchronizing signal is transmitted to a slave-mode liquid crystal drive circuit and a low side liquid crystal drive circuit. Since each column side liquid crystal drive circuit builds in Display RAM, the control circuit. etc., the control circuit of each slave liquid crystal drive circuit has

the control circuit of a master liquid crystal drive circuit, and the composition of taking a synchronization, based on the synchronizing signal from a master liquid crystal drive circuit. However, if an outpatient department noise etc. rides on a supply signal line from a master liquid crystal drive circuit and a slave liquid crystal drive circuit judges this noise to be a signal accidentally The column side liquid crystal drive output value which synchronous gap arose in actuation of the gradation arithmetic circuit of the control circuit between a master and a slave etc., and was generated from the gradation arithmetic circuit, The abnormalities in a display of the liquid crystal display panel of vertical Rhine for the output continue by the slave drive circuit where the master drive circuit and the synchronization shifted [the liquid crystal display display expressed with a difference with the low side liquid crystal drive output value outputted based on a liquid crystal gradation level signal].

[0004] The gradation level signal which such synchronous gap is generated by the control circuit of a master side, and is transmitted to a low side liquid crystal drive circuit, From the ability to judge by the comparison with the gradation level signal of a slave liquid crystal drive circuit respectively generated by the control circuit. in the conventional liquid crystal drive circuit Synchronous gap is judged in the self-test circuit in a slave liquid crystal drive circuit, and it is supposed that a system-reset signal is supplied to all slave liquid crystal drive circuits from the judged slave liquid crystal drive circuit, all the liquid crystal drive circuits by the side of a column are initialized, and synchronous gap will be canceled. However, in order to perform this initialization, the problem that a liquid crystal display display carries out a blackout for a moment arises. Hereafter, this is explained in full detail.

[0005] Drawing 12 is the block diagram showing an example of the conventional liquid crystal display. In the configuration in which three column side liquid crystal drive circuits 2-ICs 4 were established in the liquid crystal display 1 of 480x240 size, and one low side liquid crystal drive circuit IC 5 was established The liquid crystal drive circuit 2 is set as a master mode among the column side liquid crystal drive circuits 2-4, and other column side liquid crystal drive circuits 3-4 are set as a slave mode. The liquid crystal drive circuit 2 of a master mode The external resistance R1 for an oscillation is connected, and an internal oscillator is operated. Liquid crystal drive timing signal STB, the frame signal FRMB, and the gradation level signals L1 and L2 The column side slave-mode liquid crystal drive circuits 3-4, It has composition supplied to the low side liquid crystal drive circuit 5, and the self-test circuit output REFRHB has

connected mutually each column side liquid crystal drive circuits 2-4. Moreover, the CPU interface signal 7 and the system-reset signal 6 are inputted from the outside.

[0006] Next, with reference to drawing 13 , the configuration and connection relation between the master mode 2 of the column side liquid crystal drive circuits and a slave mode 3 are explained. The master mode 2 and the slave mode 3 are equipped with oscillators 13 and 23, timing generators 12 and 22, the self-test circuits 18 and 28, control circuits 14 and 24, display 15 and RAM 25, and output circuits 16 and 26.

[0007] In addition, in fact, although it becomes unnecessary [the self-test circuit 18] and becomes unnecessary [an oscillator 23 and a timing generator 22] in the column side liquid crystal drive circuit specified as the slave mode, since the same liquid crystal drive circuit is used, switches SW1-SW8 are performing these change-overs in the column side liquid crystal drive circuit specified as the master mode. In a master mode 2, if switches 1-SW 4 turn on, liquid crystal drive timing signal STB and the frame signal FRMB are outputted from a timing generator 12, these signals will be inputted into the self control circuit 14, display RAM 15 and an output circuit 16 will operate [the oscillator 13 with which the external resistance R1 for oscillators was attached will operate,]. and a liquid crystal drive output will be performed. Moreover, these signals are supplied also to the low side liquid crystal drive circuit 5 shown in a slave mode 3 and drawing 12 . Moreover, from a control circuit 14, the gradation level signals L1 and L2 are outputted, and these signals are supplied to a slave mode 3 and the low side liquid crystal drive circuit 5.

[0008] Since switches 5-SW 8 turned off the slave-mode liquid crystal drive circuit 3 and the oscillator 23 and the timing generator 22 have stopped, The signals STB and FRMB to a control circuit 24, and the signal FRMB to the self-test circuit 28 These signals were inputted from the master mode 2, the display RAM 25 and the output circuit 26 were operated, and the liquid crystal drive output was performed, and the gradation level signals L1 and L2 were outputted from the control circuit 24, and it has inputted into the self-test circuit 28 as signal L1' and L2'. As mentioned above the signals L1 and L2 to the self-test circuit 28 It is inputted from the control circuit 14 of a master mode 2, and signals L1 and L2 are compared with L1' and L2'. Consequently, while AND is carried out to the system-reset signal which the self-test circuit output REFRHB is generated, is inputted into one side of self AND circuit 27, and is inputted into another side This self-test circuit output REFRHB has composition supplied to a master mode 2 or other slave modes 4.

[0009] Next, with reference to drawing 14 , the configuration and actuation of the self-test circuit 28 are explained. If, as for the self-test circuit output REFRHB, "H" is set by "H", the set signal S performs coincidence of a signal L1, L1', and L2 and L2' by XOR 1-2 and NOR1 and any or an inequality occurs If "L" level is inputted into the data D of Philip FUROPPU FF 1 and the frame signal RRMB starts in the condition By the circuit where this output consists of a delay circuit D1, an inverter circuit INV1, NOR-circuit NOR2, an N-channel MOS transistor Nch, and a pull-up resistor RU by setting the output Q of FF1 to "L" from "H" The self-test circuit output REFRHB is constituted so that it may be set to "L" for a time delay of a delay circuit D1.

[0010] Next, with reference to drawing 15 , synchronous gap occurs in the conventional liquid crystal drive circuit, and actuation until this gap returns is explained. The operating cycle of the gradation level signals L1 and L2 first outputted by the master mode 2 is explained using drawing 15 (B). As for 1 cycle, the frame signal FRMB serves as 1 cycle in four inputs of a low pulse signal of F1-F4, and, as for liquid crystal drive timing signal STB, 121 times of standup signals are inputted between the "L" pulse of the frame signal FRMB, and the following "L" pulse.

[0011] When the "L" pulse is inputted to the timing of F1 of the first frame signal FRMB, the level of L2 is reversed with the standup signal of an STB signal until L1= "H" and L2= "H" are outputted and then the "L" pulse of F2 is inputted by the 1st standup signal of liquid crystal drive timing signal STB. Henceforth, at the time of F2, the level of L2 is reversed in the 1st standup of STB so that it may be called L1= "L" and L2= "H" at L1= "L", L2= "L", and the time of F4 at L1= "H", L2= "L", and the time of F3.

[0012] Next, in drawing 15 (A), the case where a noise (N1) rides on the frame signal FRMB is explained. The system-reset signal RESETB enters first, it has become the initialization time amount of a liquid crystal drive circuit in between for 1 cycle [2 / L1 and / L] S1, Y output serves as OFF (blackout) for flicker prevention of a liquid crystal display display, and Y output turns into a display ON output after the following cycle S2. In the ON output of S2, a noise N1 to the frame signal FRMB In and the 1 pulse ****** case Synchronous gap occurs in the standup of 3 of the following liquid crystal drive timing signal STB. Synchronous gap is detected by K6 of the detection timing K1-K11 of the self-test circuit 28, the self-test circuit output REFRHB serves as a predetermined period "L", and all the column side liquid crystal drive circuits 2-ICs 4 also including self are reset and initialized by AND-circuit 27 grade. Therefore, although the gradation level signals L1

and L2 are synchronized, in the following cycle S3, Y output becomes off and they serve as ON after the following cycle S4.

[0013]

[Problem(s) to be Solved by the Invention] When a noise rides on a frame signal as mentioned above and synchronous gap arises in the gradation level signal of a master and a slave, suppose the conventional liquid crystal drive circuit that it initializes by transmitting the self-test circuit output REFRHB which detected synchronous gap to all other column side liquid crystal drive circuits, and resetting all column side liquid crystal drive circuits, and synchronous gap is canceled. If all column side liquid crystal drive circuits are initialized, in order to prevent a flicker of Display RAM and the liquid crystal display display between the initialization time amount of a control circuit, the display off output worked, and it had troubles, like there is a possibility that it may be incorrect-judged as display failure while the blackout of the liquid crystal display display will be carried out to there being no system-reset input of normal for a moment and it became offensive to the eye.

[0014] This invention is made in order to solve this trouble, synchronous gap produces it in the gradation level signal of a master and a slave, and also while canceling this synchronous gap, it aims at offering the liquid crystal drive circuit as for which a liquid crystal display display does not carry out a blackout, and its control approach.

[0015]

[Means for Solving the Problem] As for the control approach of the liquid crystal drive circuit of this invention, a master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits where each was equipped with the control circuit which builds in a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. The gradation level signals L1 and L2 are outputted from the self control circuit 14, and it sends out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self', and said gradation level signals L1 and L2 which output L2', input into the self-test circuit

28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the control approach of the liquid crystal drive circuit which cancels synchronous gap by reversal of the logic of this signal REFRHB While the logic of said signal REFRHB is reversed, it is characterized by inserting the "H" pulse between the "L" periods of the frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and canceling synchronous gap. Therefore, it is not necessary to reset the whole system, synchronous gap can be canceled, and it is lost that the blackout of the liquid crystal display display is carried out.

[0016] Moreover, while the logic of said signal REFRHB is reversed, it is characterized by stopping the input of said frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and liquid aforementioned ****** timing signal STB, and canceling synchronous gap. Therefore, it is not necessary to reset the whole system, synchronous gap can be canceled, and it is lost that the blackout of the liquid crystal display display is carried out.

[0017] Furthermore. said signal REFRHB is inputted into said timing generator and control circuit of all column side liquid crystal drive circuits, and it is characterized by canceling synchronous gap by resetting said timing generator and said gradation level signal generator built in said control circuit. Therefore, it is not necessary to reset the whole system, synchronous gap can be canceled, and it is lost that the blackout of the liquid crystal display display is carried out.

[0018] Moreover, as for the liquid crystal drive circuit of this invention, a master mode liquid crystal drive circuit, an unit, or two or more slave-mode liquid crystal drive circuits consist of column side liquid crystal drive circuits where each was equipped with the control circuit which builds in a gradation level signal generator. While said master mode liquid crystal drive circuit generates liquid crystal drive timing signal STB and the frame signal FRMB with an oscillator 13 and a timing generator 12, inputs them into the self control circuit 14 and outputs a liquid crystal drive output This liquid crystal drive timing signal STB and the frame signal FRMB are sent out to said slave-mode liquid crystal drive circuit. It has a means to output the gradation level signals L1 and L2 from the self control circuit 14, and to send out to said slave-mode liquid crystal drive circuit. Said slave-mode liquid crystal drive circuit While inputting said liquid crystal

drive timing signal STB and the frame signal FRMB into the self control circuit 24 and outputting a liquid crystal drive output Gradation level signal L1from control circuit 24 which is self', and said gradation level signals L1 and L2 which output L2', input into the self-test circuit 28, and are inputted into this self-test circuit 28, The logic of the signal REFRHB from said self-test circuit 28 is reversed between inequalities noting that synchronous gap has arisen, when it compares [L1=L1' and] whether it is L2=L2' and these are not in agreement. In the liquid crystal drive circuit equipped with a means to cancel synchronous gap by reversal of the logic of this signal REFRHB While the logic of said signal REFRHB is reversed in said slave-mode liquid crystal drive circuit, It is characterized by having the amendment circuit which inserts the "H" pulse between the "L" periods of the frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and cancels synchronous gap. Therefore, it is not necessary to reset the whole system, synchronous gap can be canceled, and it is lost that the blackout of the liquid crystal display display is carried out.

[0019] Moreover, while the logic of said signal REFRHB is reversed in said slave-mode liquid crystal drive circuit, it is characterized by having the amendment circuit which is made to suspend the input of said frame signal FRMB inputted into said control circuit 24 from said master mode liquid crystal drive circuit, and liquid aforementioned ****** timing signal STB, and cancels synchronous gap. Therefore, it is not necessary to reset the whole system, synchronous gap can be canceled, and it is lost that the blackout of the liquid crystal display display is carried out.

[0020] Moreover, said self-test circuit 28 is characterized by equipping the last stage with an inverter. Therefore, low consumed-electric-current-ization is still attained.

[0021] Furthermore, it is characterized by having a means to input said signal REFRHB into said timing generator and control circuit of all column side liquid crystal drive circuits, to reset said timing generator and said gradation level signal generator built in said control circuit, and to cancel synchronous gap. Therefore, it is lost that it is not necessary to reset the whole system, can cancel synchronous gap, and the blackout of the liquid crystal display display is carried out by easy circuitry.

[0022]

[Embodiment of the Invention] Hereafter, the 1st operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is drawing showing an example of the equipment configuration of the liquid crystal display with which the 1st operation gestalt of this invention

is applied. For the column side liquid crystal drive circuit IC (master mode), and 3 and 4, as for the low side liquid crystal drive circuit IC and 6, in drawing 1 , the column side liquid crystal drive circuit IC (slave mode) and 5 are [1 / a liquid crystal display and 2 / a system-reset signal and 7] CPU interface signals.

[0023] In the configuration in which three column side liquid crystal drive circuits 2-ICs 4 were established in the liquid crystal display 1 of 480x240 size, and one low side liquid crystal drive circuit IC 5 was established The liquid crystal drive circuit 2 is set as a master mode among the column side liquid crystal drive circuits 2-4, and other column side liquid crystal drive circuits 3-4 are set as a slave mode. The liquid crystal drive circuit 2 of a master mode The external resistance R1 for an oscillation is connected, and an internal oscillator is operated. Liquid crystal drive timing signal STB, the frame signal FRMB, and the gradation level signals L1 and L2 The column side slave-mode liquid crystal drive circuits 3-4, It has the composition that have composition supplied to the low side liquid crystal drive circuit 5, and the CPU interface signal 7 and the system-reset signal 6 are inputted from the outside.

[0024] Next, with reference to drawing 2 , the configuration and connection relation between the master mode 2 of the column side liquid crystal drive circuits and a slave mode 3 are explained. The master mode 2 and the slave mode 3 are equipped with oscillators 13 and 23, timing generators 12 and 22, the self-test circuits 18 and 28, control circuits 14 and 24, the display rams 15 and 25, the pulse amendment circuits 19 and 29, and OR circuits or11 and or12.

[0025] In addition, in fact, although it becomes unnecessary [the self-test circuit 18 the pulse amendment circuit 19, and OR circuit or11] and becomes unnecessary [an oscillator 23 and a timing generator 22] in the column side liquid crystal drive circuit specified as the slave mode, since the same liquid crystal drive circuit is used, these change-overs are performed in the switch SW1 - SW8 grade in the column side liquid crystal drive circuit specified as the master mode. In a master mode 2, if switches 1-SW 4 turn on, liquid crystal drive timing signal STB and the frame signal FRMB are outputted from a timing generator 12, these signals will be inputted into the self control circuit 14, display RAM 15 and an output circuit 16 will operate [the oscillator 13 with which the external resistance R1 for oscillators was attached will operate,], and a liquid crystal drive output will be performed. Moreover, these signals are supplied also to the low side liquid crystal drive circuit 5 shown in a slave mode 3 and drawing 1 . Moreover, from a control circuit 14, the gradation level signals L1 and L2 are outputted.

and these signals are supplied to slave modes 3-4 and the low side liquid crystal drive circuit 5.

[0026] Since switches 5-SW 8 turned off the slave-mode liquid crystal drive circuit 3 and the oscillator 23 and the timing generator 22 have stopped, STB to a control circuit 24, and a FRMB signal Although these signals are inputted from a master mode 2, display RAM 25 and an output circuit 26 are operated and a liquid crystal drive output is performed The frame signal FRMB inputted branches to three, and one of them is inputted into one input terminal of the pulse amendment circuit 29. Other one has the composition that the output and OR of the pulse amendment circuit 29 which are inputted into one input terminal of 0R circuit or21, and are inputted into one [of this 0R circuit or21] of other input terminals are taken, it is inputted into a control circuit 24, and one of further others is inputted into the self-test circuit 28. Moreover, the gradation level signals L1 and L2 were outputted from the control circuit 24, and it has inputted into the self-test circuit 28 as signal L1' and L2'. As mentioned above, signals L1 and L2 are inputted into the self-test circuit 28 from the control circuit 14 of a master mode 2, and it has to it signals L1 and L2, L1', and the composition of L2' being compared, consequently the self-test circuit output. REFRHB being generated. and being inputted into one terminal of the pulse amendment circuit 29.

[0027] Next, with reference to drawing 3 , the configuration and actuation of the self-test circuit 28 of this operation gestalt are explained. If "H" is set to the self-test circuit output REFRHB by "H", the set signal S performs coincidence of a signal L1, L1', and L2 and L2' by XOR 1-2 and NOR1 and any or an inequality occurs If "L" level is inputted into the data D of Philip FUROPPU FF 1 and the frame signal FRMB starts in the condition By the circuit where the signal consists of a delay circuit D1, an inverter circuit INV1, NOR-circuit NOR2, and an inverter circuit INV2 by setting the output Q of FF1 to "L" from "H" The self-test circuit output REFRHB is constituted so that it may become a part for the time delay of a delay circuit D1 "L." That is, it changes to the Nch transistor of the conventional self-test circuit shown in drawing 14 , and the inverter circuit INV2 is used. This is because it is necessary to initialize no column side liquid crystal drive circuits so that it may mention later.

[0028] Next, with reference to drawing 4 , the configuration and actuation of the pulse amendment circuit 29 of this operation gestalt are explained. It is initialized by the reset signal RB and, as for the amendment circuit output FRPW. "L" is set. If the self-test circuit output REFRHB of drawing 3 is inputted and Q

output of FF10 is set to "H" from "L" in falling of the following frame signal FRMB at the time of the standup of the frame signal FRMB It has the composition that the "H" pulse signal for a time delay of a delay circuit D30 (PW1) is outputted from the amendment output FRPW after a part for the time delay Dy 1 of a delay circuit D20, by the delay circuit D20, the delay circuit D30, the inverter circuit INV10, and AND-circuit AND10.

[0029] Next, with reference to drawing 5 , synchronous gap occurs in the liquid crystal drive circuit of this operation gestalt, and actuation until this gap returns is explained. The operating cycle of the gradation level signals L1 and L2 first outputted by the master mode 2 is explained using drawing 5 (B). As for 1 cycle, the frame signal FRMB serves as 1 cycle in four inputs of a low pulse signal of F1-F4, and, as for liquid crystal drive timing signal STB, 121 times of standup signals are inputted between the "L" pulse of the frame signal FRMB, and the following "L" pulse.

[0030] When the "L" pulse is inputted to the timing of F1 of the first frame signal FRMB, the level of L2 is reversed with the standup signal of an STB signal until L1= "H" and L2= "H" are outputted and then the "L" pulse of F2 is inputted by the 1st standup signal of liquid crystal drive timing signal STB. Henceforth, at the time of F2, the level of L2 is reversed in the 1st standup of STB so that it may be called L1= "L" and L2= "H" at L1= "L", L2= "L", and the time of F4 at L1= "H", L2= "L", and the time of F3.

[0031] Next, in drawing 5 (A), the case where a noise (N1) rides on the frame signal FRMB is explained. The system-reset signal RESETB enters first, it has become the initialization time amount of a liquid crystal drive circuit in between for 1 cycle [2 / L1 and / L] S1, Y output serves as OFF (blackout) for flicker prevention of a liquid crystal display display, and Y output serves as ON after the following cycle S2. In the ON output of S2, synchronous gap occurs [a noise N1] 1 pulse ****** case to the frame signal FRMB in the standup of 3 of the following liquid crystal drive timing signal STB. And by K6 of the detection timing K1-K10 of the self-test circuit 28 In falling of the frame signal FRMB which it becomes L1 !=L1', and the "L" pulse signal occurs in the output REFRHB of the self-test circuit 28, is inputted into one side of the own pulse amendment circuit 29, and is inputted into other one side of this pulse amendment circuit 29 As shown in (PW1) of drawing 4 (B), the "H" pulse signal for a time delay of a delay circuit D30 occurs in the pulse amendment circuit output FRPW. The this "H" pulse is inputted into OR circuit or21 with the frame signal FRMB. The "H" pulse is added to the frame signal FRMB inputted into the

control circuit 24 which is the output of this OR circuit or21 +one time. Although it progresses +one and signal L1' and L2' are set to "L" and "L" from the condition that the condition of the cycle of the gradation level signal of the own control circuit 24 is the cycle of the gradation level signal of a master mode 2 L1!=L1' and since the synchronization has still shifted from L2 !=L2', to the following timing of K7 in falling of F4 of the frame signal FRMB The "H" pulse is again added +one time from the pulse amendment circuit 29 (PW2), and from the pulse amendment circuit 29, the "H" pulse is added +one (PW3), and is synchronized until it does in this way and can take a synchronization to the timing of K9. Therefore, without resetting which column side liquid crystal drive circuits 2-4, Y output turns into a display ON output, and it can avoid that a blackout is carried out also until it can cancel synchronous gap and synchronizes.

[0032] Next, the 2nd operation gestalt of this invention is explained with reference to a drawing. The liquid crystal display with which the liquid crystal drive circuit of this 2nd operation gestalt is applied is the same as the liquid crystal display shown in drawing 1 , and that explanation is omitted. So that drawing 6 may be drawing showing the 2nd [this] configuration and connection relation of the master mode 2 and slave mode 3 in an operation gestalt and it may mention later by drawing 7 by OR circuits or21 and or22 with the configuration of the pulse amendment circuit 29 It is the same as that of the configuration of the 1st operation gestalt shown in drawing 2 except for the point which has the composition that OR of liquid crystal drive timing signal STB and the frame signal FRMB which are inputted from a master mode 2 is carried out to the output MASK of the pulse amendment circuit 29, and they are inputted into a control circuit 24. Moreover, it is the same as that of the 1st operation gestalt which also shows the configuration and actuation of the self-test circuit 28 to drawing 3 , and these explanation is omitted.

[0033] Next, with reference to drawing 7 , the configuration and actuation of a pulse amendment circuit in this operation gestalt are explained. It is initialized by the reset signal RB, and the pulse amendment circuit output MASK is in the "L" condition, and it is constituted so that it may be "L" of the self-test circuit output REFRHB, the pulse amendment circuit output MASK may be set to "H" and the pulse amendment circuit output MASK may be set to "L" from "H" in the standup of the following frame signal FRMB.

[0034] Next, with reference to drawing 8 , synchronous gap occurs in the liquid crystal drive circuit of this 2nd operation gestalt, and actuation until this gap

returns is explained. In addition, about the operating cycle of the gradation level signals L1 and L2 outputted by the master mode 2 shown in drawing 8 (B), since it is the same as that of the 1st operation gestalt shown in drawing 5 (B), the explanation is omitted. Next, in drawing 8 (A), the case where a noise (N1) rides on the frame signal FRMB is explained. The system-reset signal RESETB enters first, it has become the initialization time amount of a liquid crystal drive circuit in between for 1 cycle [2 / L1 and / L] S1, Y output serves as OFF (blackout) for flicker prevention of a liquid crystal display display, and Y output serves as ON after the following cycle S2. In the ON output of S2, synchronous gap occurs [a noise N1] 1 pulse ****** case to the frame signal FRMB in the standup of 3 of the following liquid crystal drive timing signal STB. And by K6 of the detection timing K1-K10 of the self-test circuit 28 Become L1 !=L1' and the "L" pulse signal occurs in the output REFRHB of the self-test circuit 28. It is inputted into one side of the own pulse amendment circuit 29, and the output MSAK of this pulse amendment circuit 29 is set to "H." The output of each OR circuit or21 and or22 is set to "H", and the clock of liquid crystal drive timing signal STB and the frame signal FRMB inputted from a master mode 2 is not inputted into a control circuit 24. If a synchronization is henceforth established to the timing of K7 and the output REFRHB of the self-test circuit 28 is set to "H", the output MSAK of the pulse amendment circuit 29 will be set to "L", the clock of liquid crystal drive timing signal STB from a master mode and the frame signal FRMB will be inputted into a control circuit 24, and it will return to the usual actuation. Therefore, without resetting which column side liquid crystal drive circuits 2-4, Y output turns into a display ON output, and it can avoid that a blackout is carried out also until it can cancel synchronous gap and synchronizes.

[0035] Next, the 3rd operation gestalt of this invention is explained with reference to a drawing. The liquid crystal display with which this 3rd operation gestalt is applied is the same as that of drawing 12 explained as a conventional technique, and that explanation is omitted. Drawing 9 is drawing showing the 3rd [this] configuration and connection relation of the master mode 2 and slave mode 3 in an operation gestalt, and that configuration is the same as that of the configuration of the conventional technique shown in drawing 13 except for the point of being inputted into the control circuit 24 as it is, without the self-test circuit output REFRHB and a system reset signal minding an AND circuit, and the point that the output REFRHB of a self-test circuit is inputted into each timing generator 12.

[0036] Drawing 10 is drawing showing the connection relation of the gradation level signal generator 31 built in the control circuit 24 of this 3rd operation gestalt. The gradation level signal generator 31 is a circuit which generates the cycle of actuation of drawing 11 (B) of L1 and L2, is initialized in the AND logic of the output REFRHB of a system-reset signal and a self-test circuit, and will be in the condition of signal L1= "H" and L2= "H" in the standup of the following liquid crystal drive timing signal STB (F1 of drawing 11 (B)).

[0037] Next, in drawing 11 (A), the case where a noise (N1) rides on the frame signal FRMB is explained. The system-reset signal RESETB enters first, it has become the initialization time amount of a liquid crystal drive circuit in between for 1 cycle [2 / L1 and / L] S1, Y output serves as OFF (blackout) for flicker prevention of a liquid crystal display display, and Y output serves as ON after the following cycle S2. In the ON output of S2, synchronous gap occurs [a noise N1] 1 pulse ****** case to the frame signal FRMB in the standup of 3 of the following liquid crystal drive timing signal STB. And by K6 of the detection timing K1-K11 of the self-test circuit 28 Become L1 !=L1' and the "L" pulse signal occurs in the output REFRHB of the self-test circuit 28. Although this self-test output REFRHB is inputted into an own control circuit 24 and an own timing generator 22 and also the gradation level signal generator 31 which was inputted into all other column side liquid crystal drive circuits, and was built in each timing generator and control circuit is reset To other control circuits of each control circuit, "H" of a system-reset signal continues as it is, and is maintained to them. Therefore, it can avoid now that Y output turns into a display ON output, and the blackout of it is carried out also until the display action of which column side liquid crystal drive circuits 2-4 can cancel synchronous gap and is synchronized, without being reset.

[0038]

[Effect of the Invention] The following effectiveness produces the liquid crystal drive circuit and its control approach of this invention in it being constituted and operating, as explained above. Since it considered as the configuration which synchronizes without using a system-reset function when synchronous gap occurred and synchronous gap was canceled, the blackout of a liquid crystal display display can be lost. Moreover, in the 1st operation gestalt and the 2nd operation gestalt, it is necessary to write as the configuration which synchronizes for liquid crystal drive circuit itself which synchronous gap produced, and to initialize no column liquid crystal drive circuits IC, the self-test circuit output REFRHB line which connects between each column liquid crystal drive circuit

IC can be omitted, and simplification of a liquid crystal display can be attained. Since the Nch open drain of the REFRHB terminal for furthermore initializing all the column liquid crystal drive circuits IC becomes unnecessary, there is effectiveness, like further low consumed-electric-current-ization can be attained (for example, when it is eight VGA sizes, penetration current MAX5mA of a throughout can be reduced at the time of reset).

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing an example of the equipment configuration of the liquid crystal display with which the 1st operation gestalt of this invention is applied.

[Drawing 2] It is drawing for explaining the 1st operation gestalt of this invention.

[Drawing 3] It is drawing for explaining the configuration and actuation of the self-test circuit 28 of this operation gestalt.

[Drawing 4] It is drawing for explaining the configuration and actuation of the 1st of the pulse amendment circuit 29 of an operation gestalt which are shown in drawing 2 .

[Drawing 5] It is drawing for explaining the synchronous gap dissolution actuation in the 1st operation gestalt.

[Drawing 6] It is drawing for explaining the 2nd operation gestalt of this invention.

[Drawing 7] It is drawing for explaining the configuration and actuation of the 2nd of the pulse amendment circuit 29 of an operation gestalt which are shown in drawing 6 .

[Drawing 8] It is drawing for explaining the synchronous gap dissolution actuation in the 2nd operation gestalt.

[Drawing 9] It is drawing for explaining the 3rd operation gestalt of this invention.

[Drawing 10] It is drawing showing the connection relation of the gradation level signal generator in the 3rd operation gestalt.

[Drawing 11] It is drawing for explaining the synchronous gap dissolution actuation in the 3rd operation gestalt.

[Drawing 12] It is drawing showing an example of the liquid crystal display with which the conventional liquid crystal drive circuit is applied.

[Drawing 13] It is drawing for explaining the conventional liquid crystal drive circuit.

[Drawing 14] It is drawing for explaining the conventional configuration and actuation of the self-test circuit 28 of a liquid crystal drive circuit.

[Drawing 15] It is drawing for explaining the synchronous gap dissolution actuation in the conventional liquid crystal drive circuit.

[Description of Notations]

1 Liquid Crystal Display
2 Column Side Liquid Crystal Drive Circuit IC (Master Mode)
3-4 Column side liquid crystal drive circuit IC (slave mode)
5 Low Side Liquid Crystal Drive Circuit IC
6 System-Reset Signal
7 CPU Interface Signal
12 22 Timing generator
13 23 Oscillator
14 24 Control circuit
15 25 Display ram
17, 27, AND10, AND20, AND30, AND40 AND circuit
18 28 Self-test circuit
19 29 Pulse amendment circuit
31 Gradation Level Signal Generator
or11, or12, or21, or22 OR circuit
XOR1, XOR2 XOR circuit
NOR1, NOR2 NOR circuit
FF1, FF10, FF11, a flip-flop
INV1, INV2, INV10 Inverter circuit
D1, D10, D11, D20, D30 Delay circuit
Nch N-channel MOS transistor
DOOFB' Display FU output
STB Liquid crystal drive timing signal
FRMB Frame signal
L1, L2 Master mode gradation level signal
L1', L2' Slave-mode gradation level signal
REFRHB Self-test circuit output
RESETB System-reset signal
FRPW, MASK Pulse amendment circuit output
N1 Noise
S1-4 Operating cycle of L1 and L2
K1-K11 Self-test detection timing
PW 1-3 Pulse amendment circuit output
Y output Liquid crystal drive output